VII EMC Front End Electronics

VII.1 Overview

The STAR barrel electromagnetic calorimeter (EMC) is a lead-scintillator sampling calorimeter located inside the STAR magnet as shown schematically in Fig. VII.1. The barrel calorimeter covers $-1 \le \eta \le 1$ and $0 \le \phi \le 2\pi$. The barrel has 4800 towers giving a segmentation of $(\Delta\eta, \Delta\phi) = (0.05, 0.05)$.

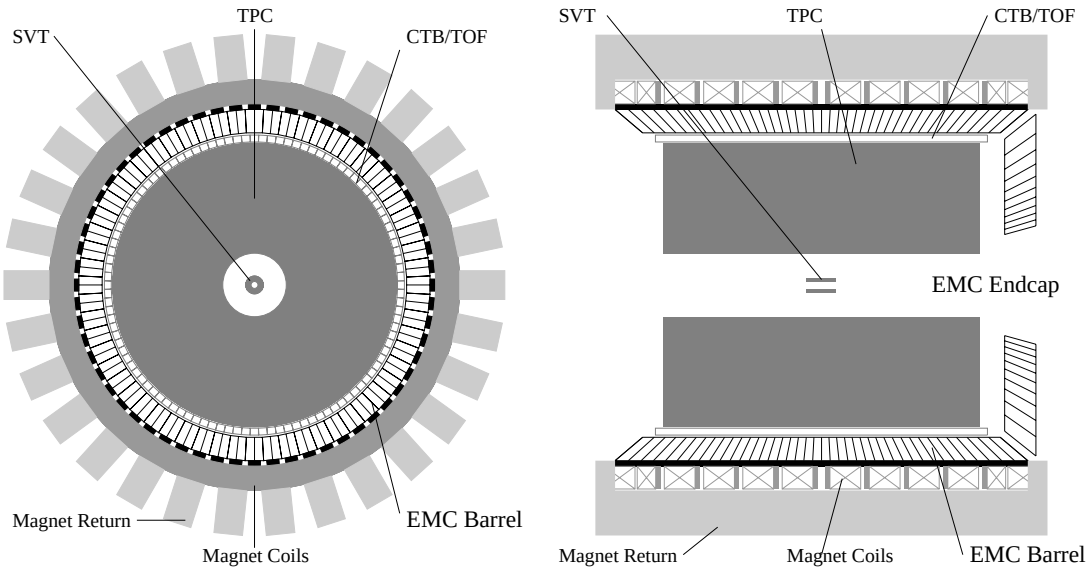


Fig. VII.1. Schematic end view and side view of the STAR EMC showing the EMC Barrel and EMC Endcap.

The EMC is 19 radiation lengths (X_o) deep. The calorimeter is composed of 21 layers of 5-mm thick scintillator alternated with 5-mm thick lead converters. The scintillator tiles are read-out with wavelength-shifting fibers coupled with clear fibers connected to photomultiplier tubes (PMT) located outside the magnet. A shower maximum detector (SMD) is located at a depth of 5 X_o that provides high spatial resolution. The SMD is a gas/strip counter composed of 1200 patches of (15,15) strips in (η, ϕ) giving a spatial resolution of $(\Delta\eta, \Delta\phi) = (0.007, 0.007)$ and 36,000 total strips.

The EMC is arranged in 120 modules each covering $(\Delta\eta, \Delta\phi) = (1.0, 0.1)$. Each module contains 40 towers and 1 SMD chamber as shown schematically in Fig. VII.2. In total, there are 4800 channels of PMT signals for the towers and 36,000 channels of strip signals for the SMD. A schematic drawing of the layout of the strips for the SMD is shown in Fig. VII.3.

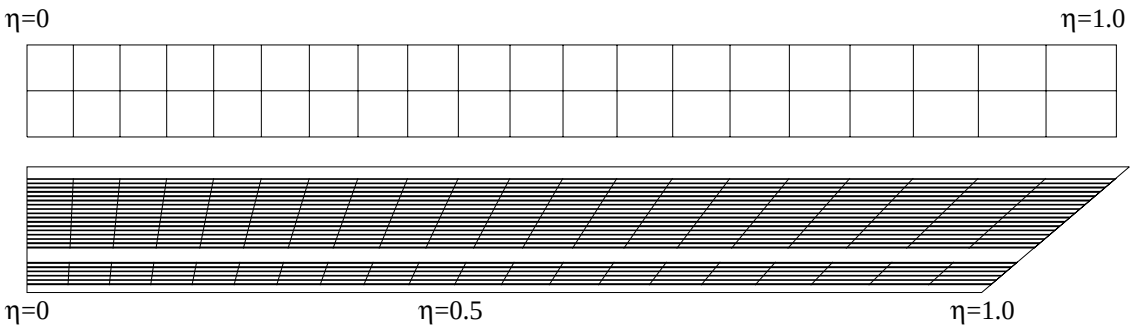


Fig. VII.2. Schematic drawing of one STAR EMC module showing a side view of the module and a top view of the last layer of tiles in the towers.

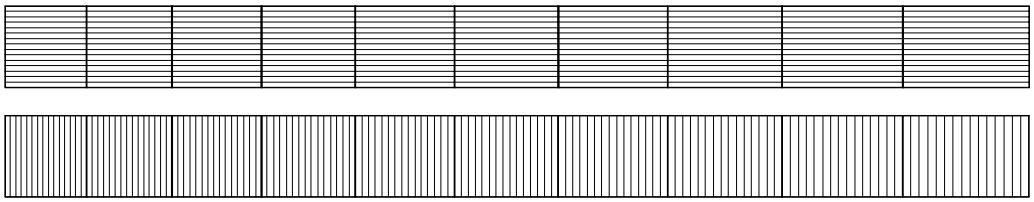


Fig. VII.3. Schematic top view of shower maximum detector showing 10 groups of strips. Each group of strips contains 15 strips in η and 15 strips in ϕ. Each SMD module thus has 300 signals.

For the tower readout, there are 30 electronics crates mounted on the back-leg iron of the STAR magnet. These crates include the digitization of the PMTs and generation of level 0 trigger information. For the SMD, the electronics is mounted on the end ($|\eta| = 1$) of each of the 120 EMC modules which are connected to 8 SMD readout modules mounted on the end of the magnet. The location of the EMC electronics is shown schematically in Fig. VII.4.

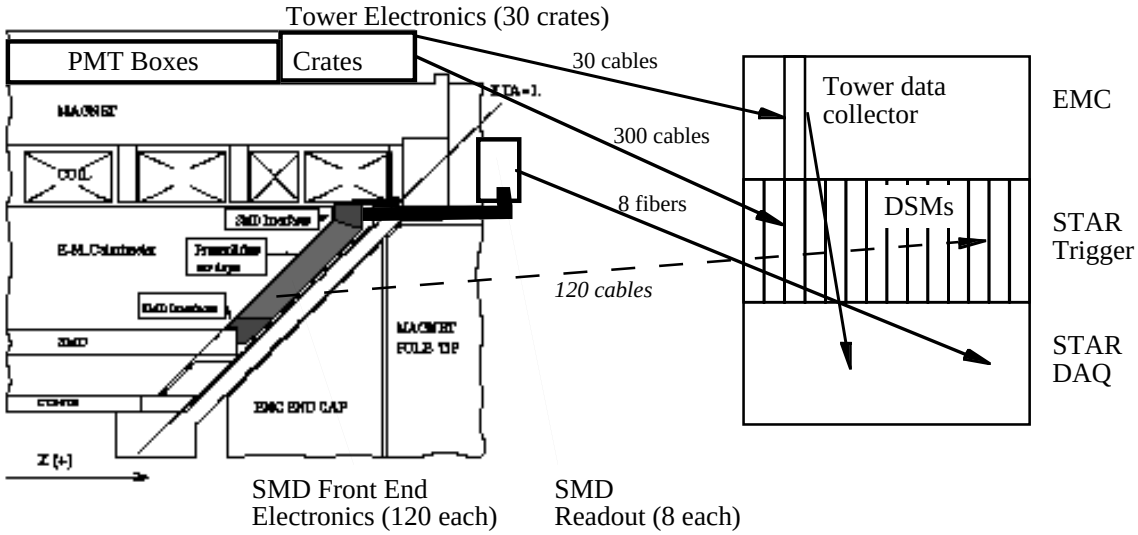


Fig. VII.4. Conceptual layout of EMC electronics showing the tower electronics on the magnet backlegs, the SMD front end electronics on the end of the EMC modules, and the SMD readout located on the end of the STAR magnet.

VII.2 EMC Electronics

The electronics for the STAR EMC (Fig. VII.5) are designed to take physics data from the tower PMTs and the SMD. The electronics interacts with slow controls to read and set control parameters, sends the data to STAR DAQ, and produces a fast level 0 trigger. The EMC electronics reads all parameters for every crossing in synch with the RHIC clock.

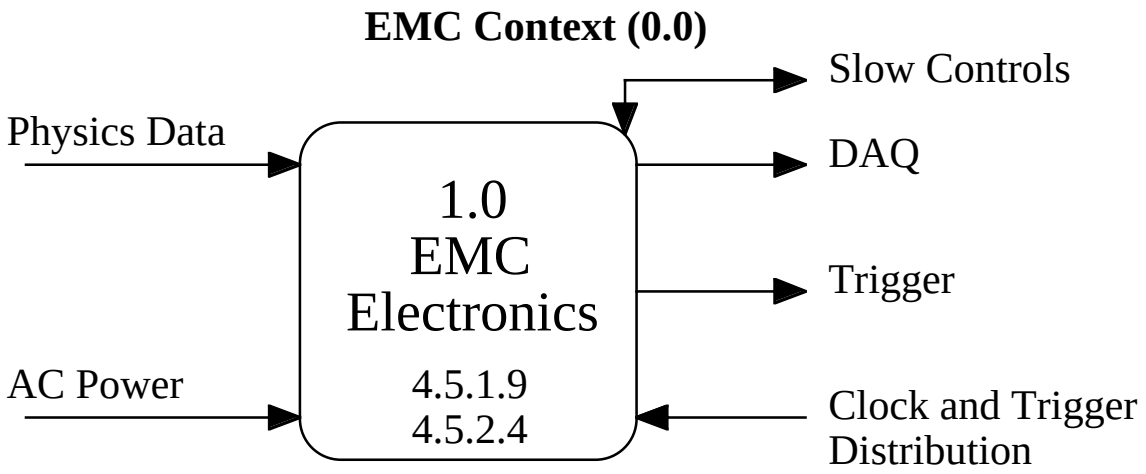


Fig VII.5. Context Diagram for STAR EMC Electronics

Part of the EMC electronics resides on the STAR magnet and part resides on the platform as shown in Fig. VII.6. The tower electronics are located in 30 crates mounted on the back-legs of the STAR magnet. These crates send their data over 30 twisted pair cables to the EMC data collector located on the platform. These crates also send level 0 trigger information to the STAR trigger on 300 twisted pair cables. The tower data collector collects the data from the crates and sends it to STAR DAQ. The SMD electronics is located on the $\eta = 1$ ends of the 120 EMC modules. These 120 sets of SMD electronics are readout with 8 SMD readout modules mounted on the end of STAR magnet. These SMD readout modules send their data to DAQ over 8 fibers.

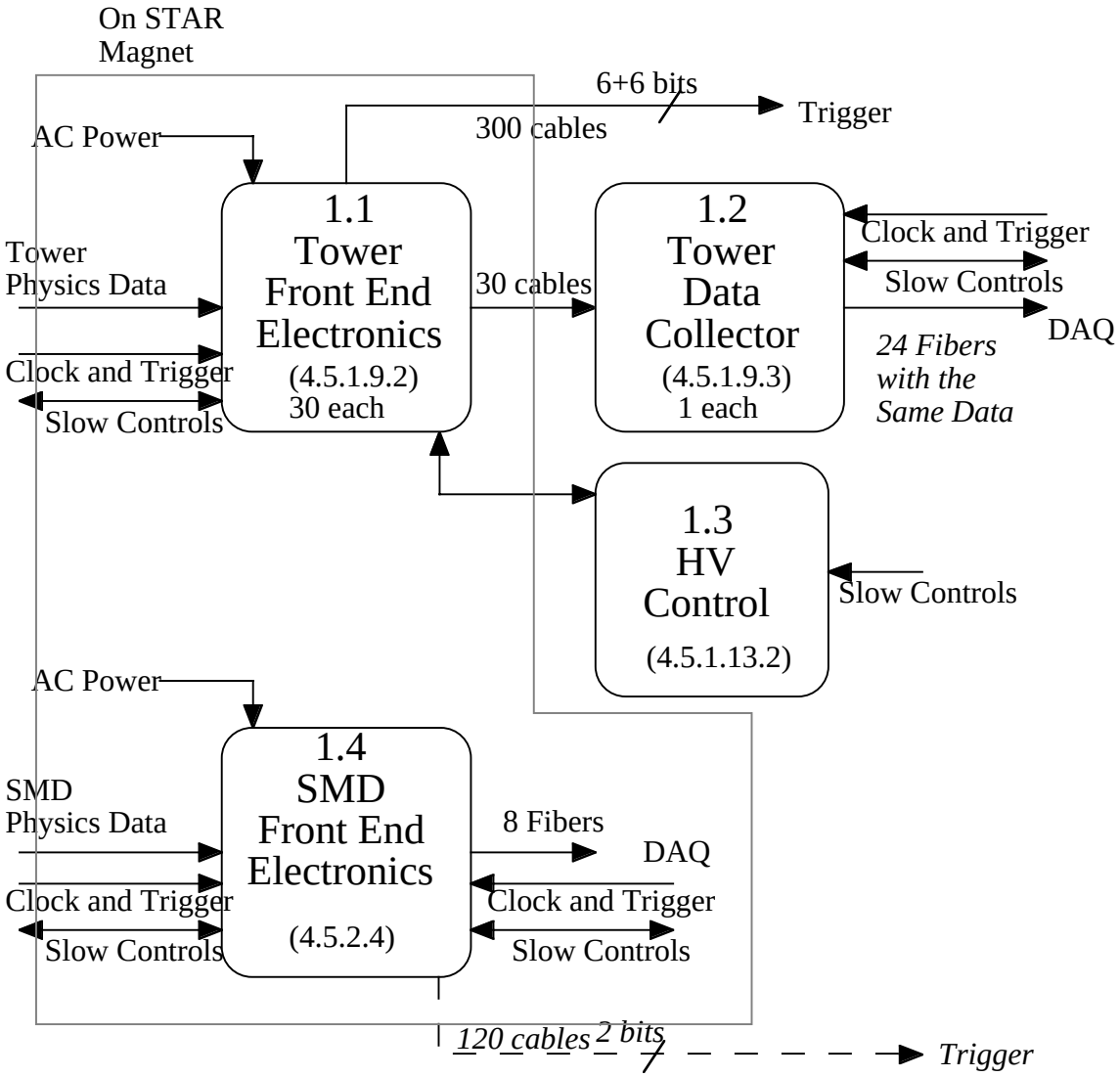


Fig.VII.6. Diagram showing the EMC electronics on the magnet and the EMC data collectors on the platform.

VII.2.1 Tower Electronics

Each of the tower electronics crates (Fig. VII.7) reads out 160 tower PMTs. In each crate there are 10 tower front-end electronics cards. Each card handles 32 channels of PMT signals. LEDs drivers are located in the tower electronics crates to provide calibration. These LEDs can be turned on to produce various patterns of PMT signals. The tower crate controller contains the interface to the RHIC clock and STAR trigger distribution. The controller takes data from the 10 tower digitizer cards and sends the data to the tower data collector. Thecontroller also contains the interface to slow controls. The tower digitizer also produces level 0 trigger information in the form of 300 trigger towers $(\Delta\eta, \Delta\phi) = (0.2, 0.2)$ and 300 high towers $(\Delta\eta, \Delta\phi) = (0.05, 0.05)$.

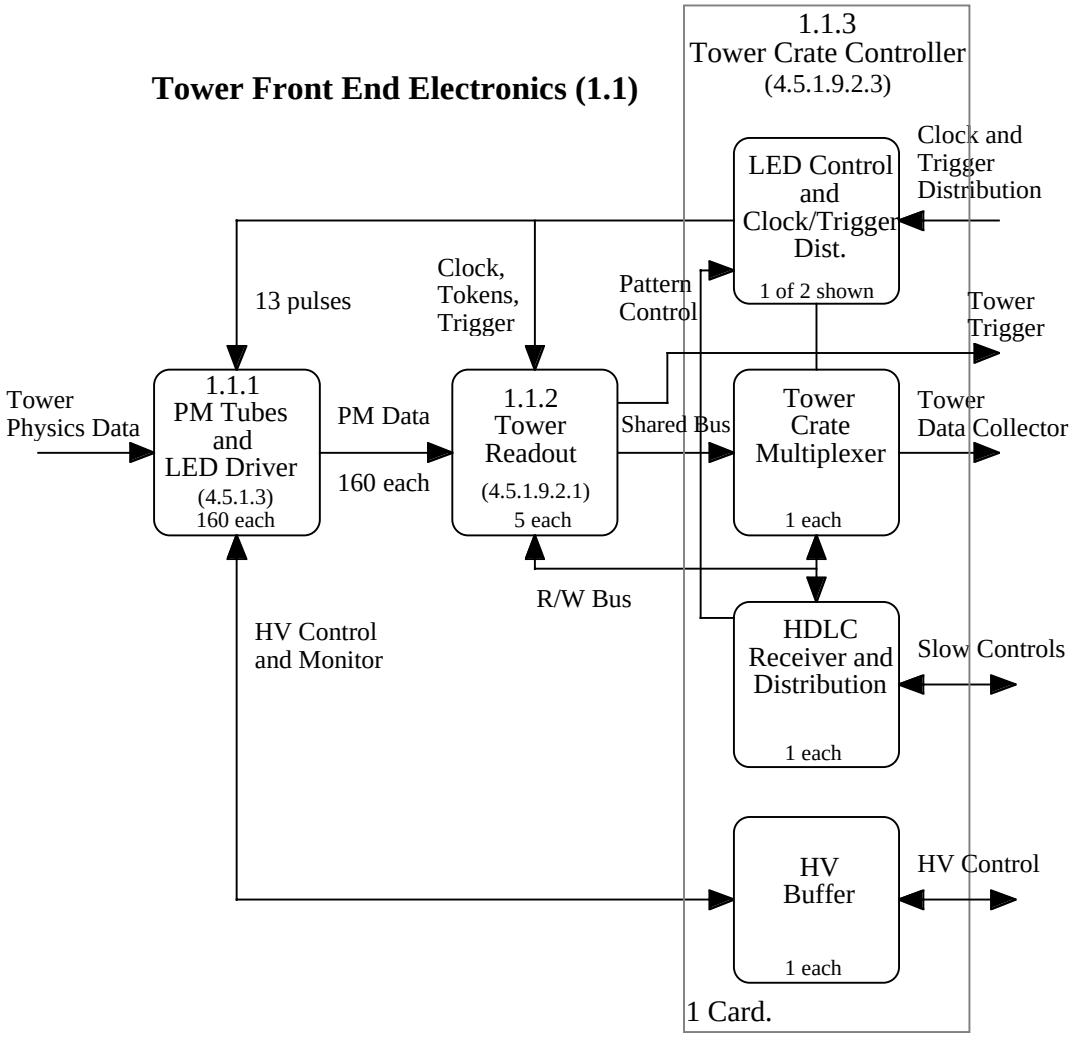


Fig. VII.7 Diagram of the tower electronics crate. This crate contains 10 tower digitizer cards and 1 controller card.

The tower electronics crates reside on the STAR magnet backlegs. There is a crate located near the $|\eta| = 1$ end of every other backleg. These crates are located next to the PMT boxes. Each electronics crate services 4 EMC modules. Each PMT box services 2 EMC modules. The fibers from the tiles of the EMC are routed through the STAR magnet structure to the PMT boxes.

The LED controller can produce 2^{13} different patterns of LEDs to test the tower electronics. The 13 different LED drivers each drive 1 LED connected optically to 7 PMTs. The HV for the PMTs is produced using Cockroft/Walton bases using a low voltage DC current. The set point and read-back of the voltages is accomplished using slow controls through an HDLC interface. The voltages are read with an ADC located in the HV control system.

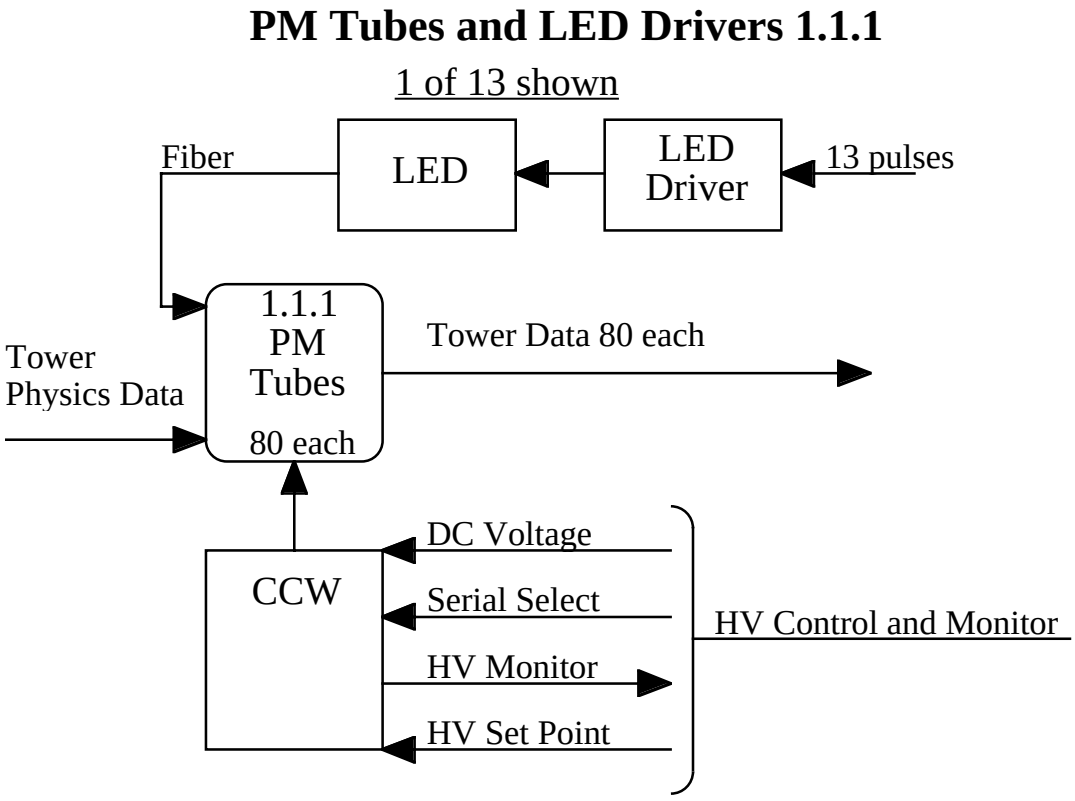


Fig. VII.8. Schematic diagram for the PMT HV supply and LED controller.

The tower digitizer card digitizes the PMT signal using a gated integrator and a 10 bit ADC. There is an integrator and ADC for each channel. The integrator system can be checked using a charge injection system. This system uses a 10 bit DAC to produce a linearity check of the integrator and ADC.

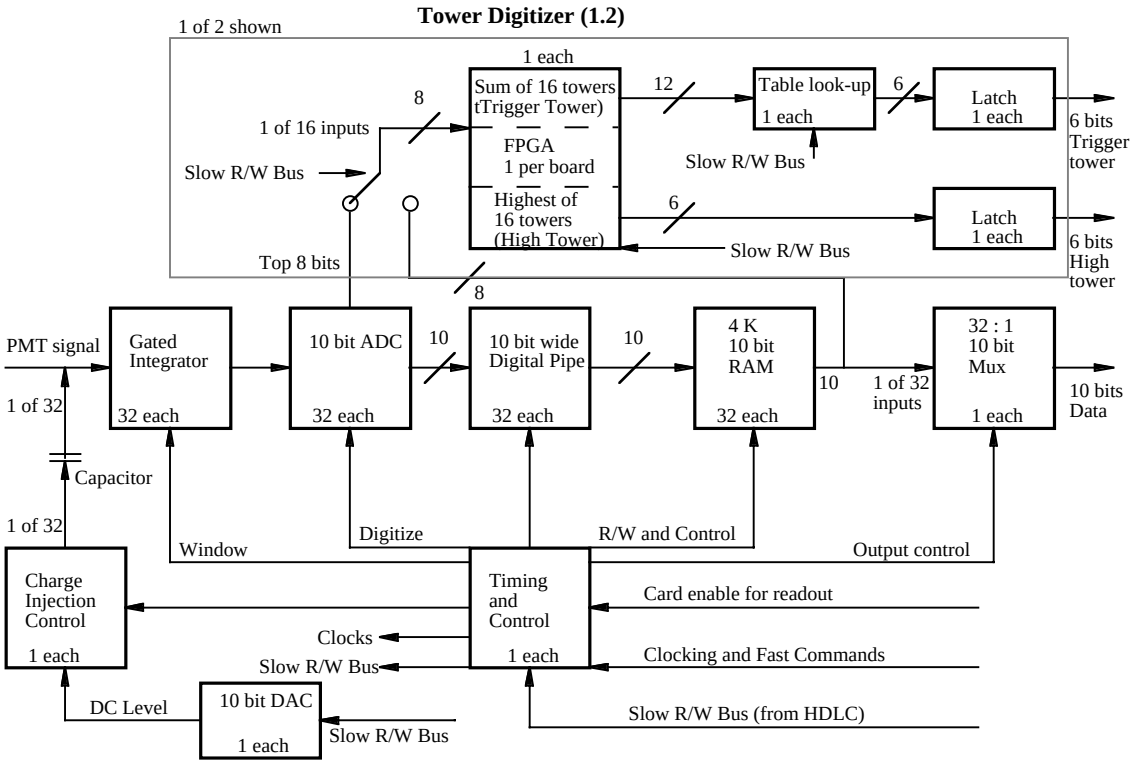


Fig. VII.10. Tower digitizer card located in the tower electronics crate.

The 10 bit output from the ADC is sent to a 10 bit wide digital pipeline to allow time for the Level 0 decision. Upon receipt of the Level 0 trigger, the ADC values are copied to a 10 bit memory with 4096 locations corresponding to the number of available trigger tokens. These data values are then sent to the tower data collector through the tower crate multiplexer. Each digitizer card handles 32 PMTs and is read-out through a single crate multiplexer to the tower data collector.

Tower Crate Controller (1.1.3)

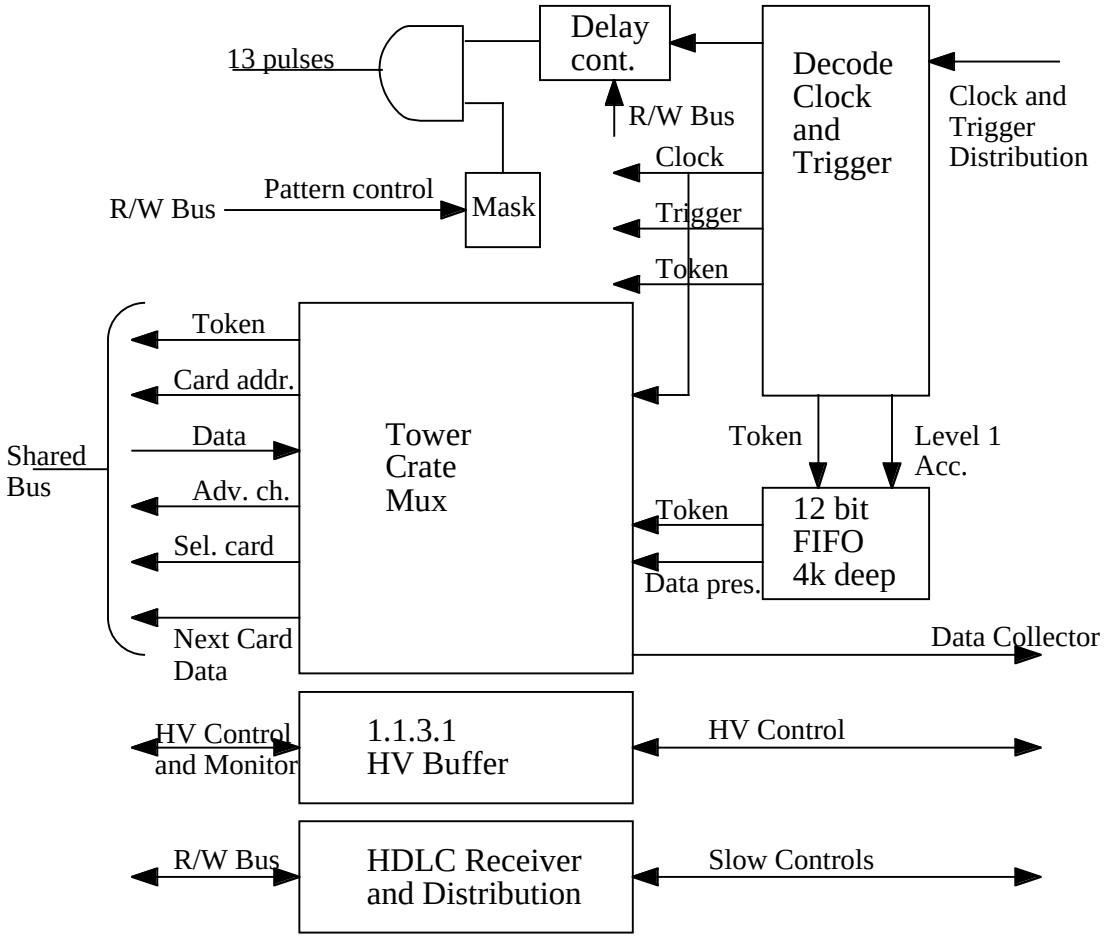


Fig. VII.11. Schematic diagram of the tower electronics multiplexer card.

The tower crate controller card has an HDLC interface to slow controls. The LED pulser system is programmed through this interface. The controller card takes the 10 bit data from a shared bus and sends the information 1 nibble at a time over twisted pair cables to the tower electronics data collector. The controller uses the trigger token from the FIFO to address the data from the tower cards.

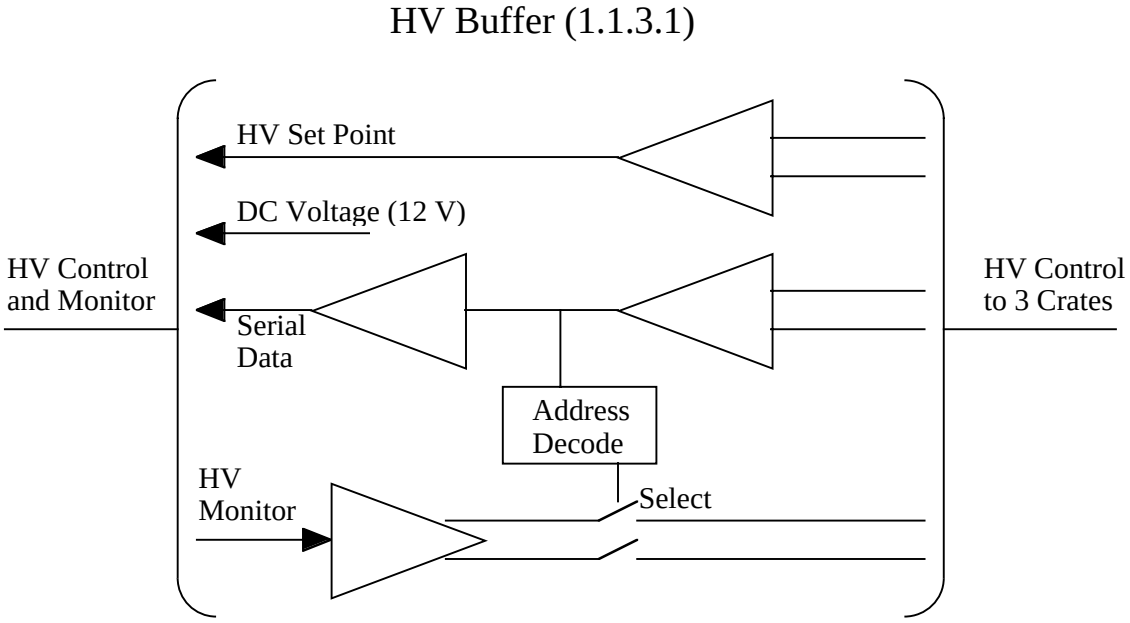


Fig. VII.12. Schematic diagram for high voltage control and monitoring.

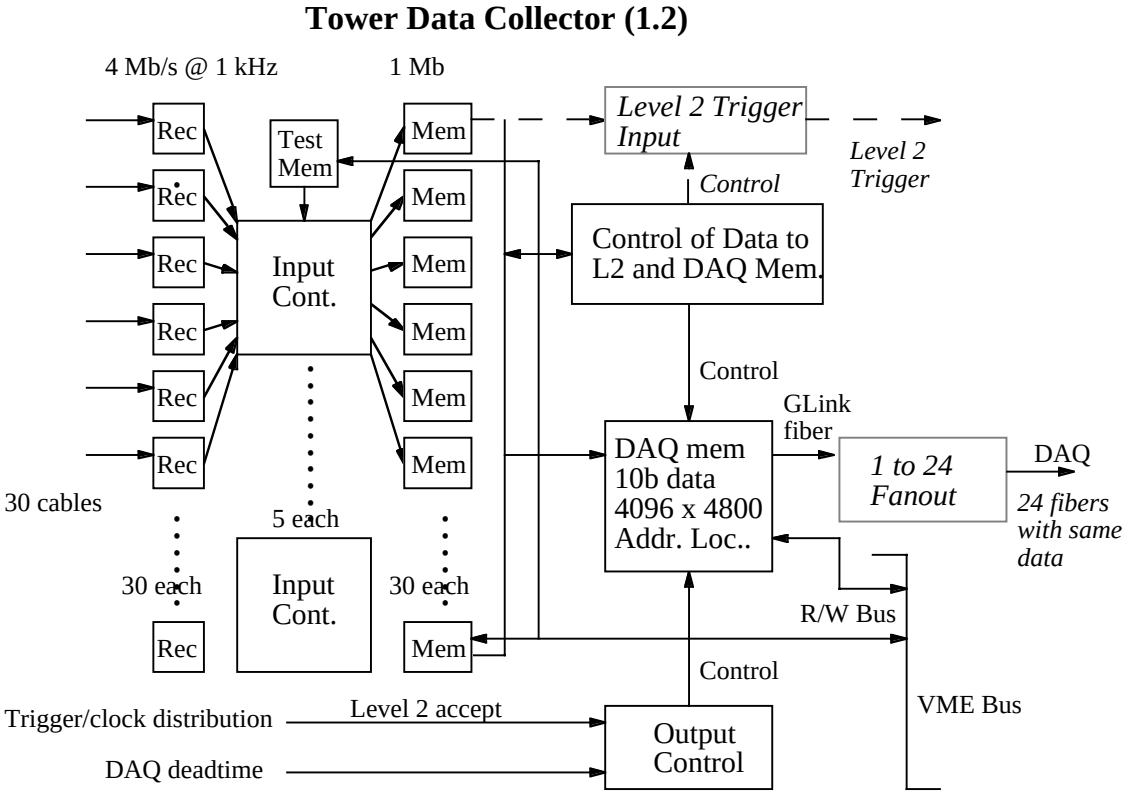


Fig. VII.13. Schematic diagram of the tower electronic data collector.

The tower electronics data collector takes the digital data from the 30 tower electronics crates and derandomizes the information into 1 Mb memories. The data collector then stores the data in a memory designed to handle 4096 x 4800 locations of 10

bit data corresponding to the 4096 trigger tokens and the 4800 tower channels. On the receipt of a Level 2 accept, the data collector sends this information to STAR DAQ. In addition, the data collector can provide the same information to the Level 2 trigger.

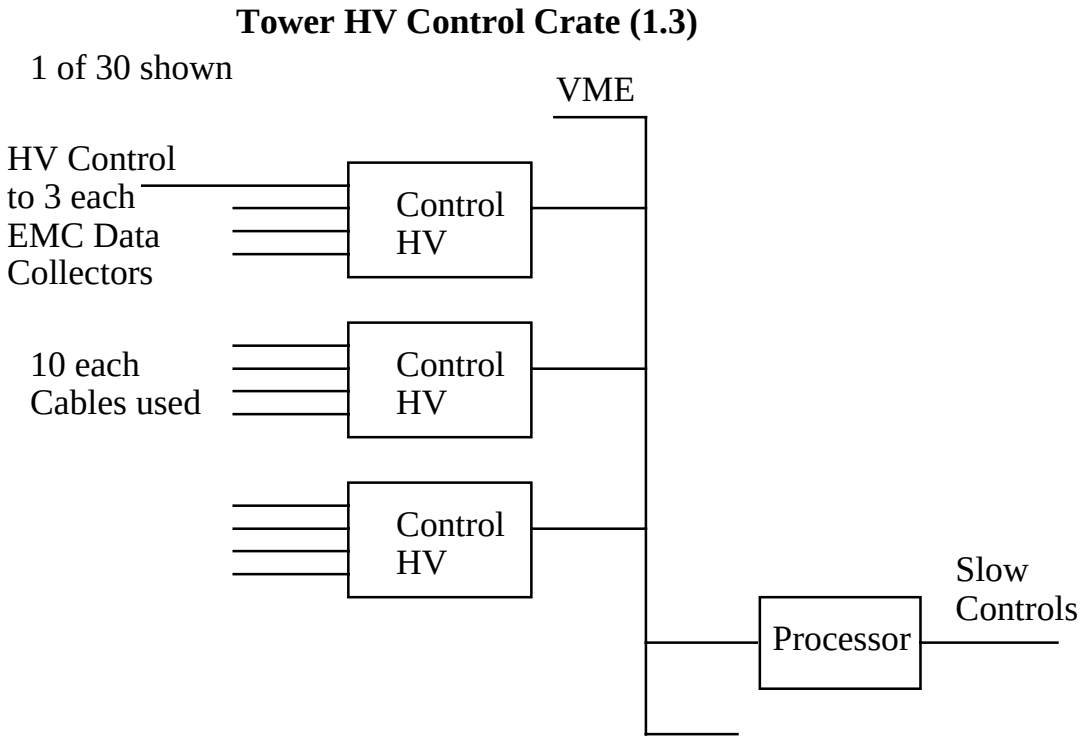


Fig. VII.14. Schematic diagram of tower high voltage crate.

VII.2.2 SMD Electronics

The overall layout of the SMD electronics is shown schematically in Fig. VII.15.

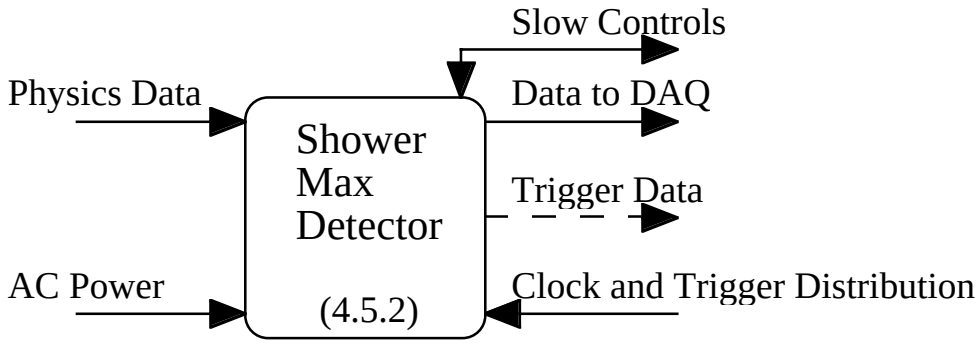


Fig. VII.15. Context diagram for SMD electronics.

The SMD Electronics receive signals from the wire chamber, digitize the signals and pass the data to DAQ over fiber optic links as shown schematically in Fig. VII.16. STAR clock and trigger signals are received and used to create all timing and control signals needed by the SMD electronics. SMD conventional systems provide high voltage

for the wire chamber. An interface to STAR Slow Controls allows the control and monitoring of the high voltage. An interface to the STAR safety system provides interlocks for the high voltage. EMC Calibration Systems provide a serial link for configuring a charge injection calibration of the SMD electronics as well as a calibration pulse, timed to match data acquisition.

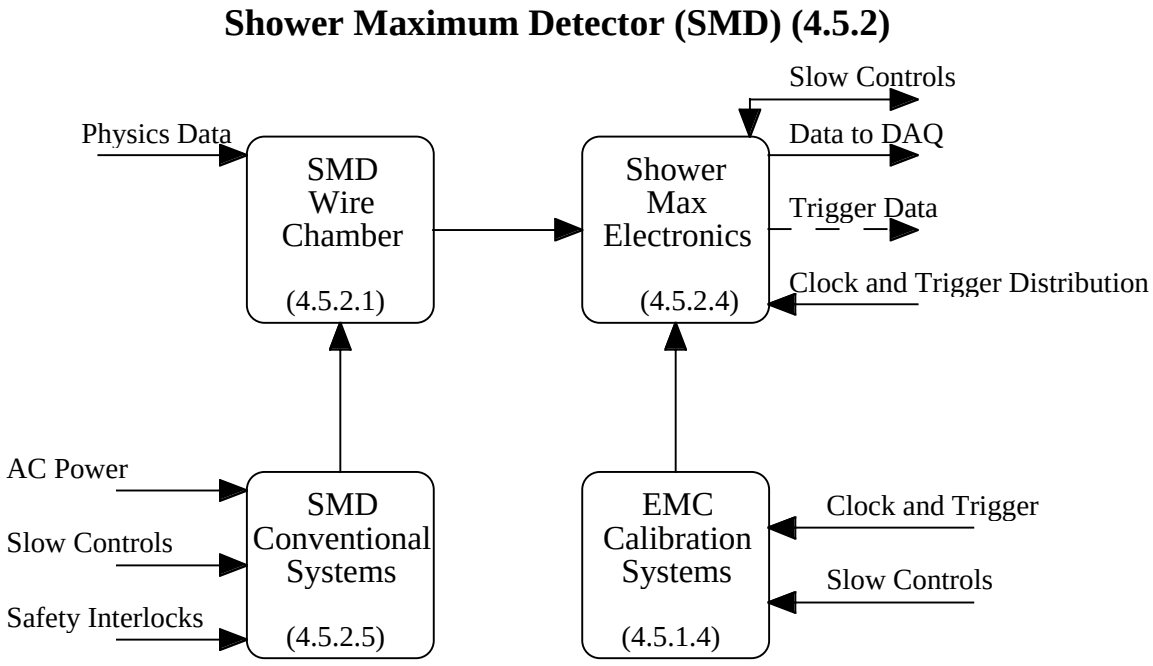


Fig. VII.16. Layout of SMD electronics.

One hundred twenty Front End Electronics cards (FEE) receive the wire chamber signals which are preamplified, shaped and stored in switched capacitor arrays. When a level 0 trigger is received, the stored data are multiplexed out of the SCAs and sent to the Read Out Modules (RDO) via twisted pair cables. Eight RDOs digitize the data and create data packets which are sent to the Data Acquisition System (DAQ) via standard STAR fiber optic links. SMD clock and timing electronics provide the appropriate timing and control signals in response to trigger commands from the Trigger system. The layout of the SMD electronics is shown in more detail in Fig. VII.17.

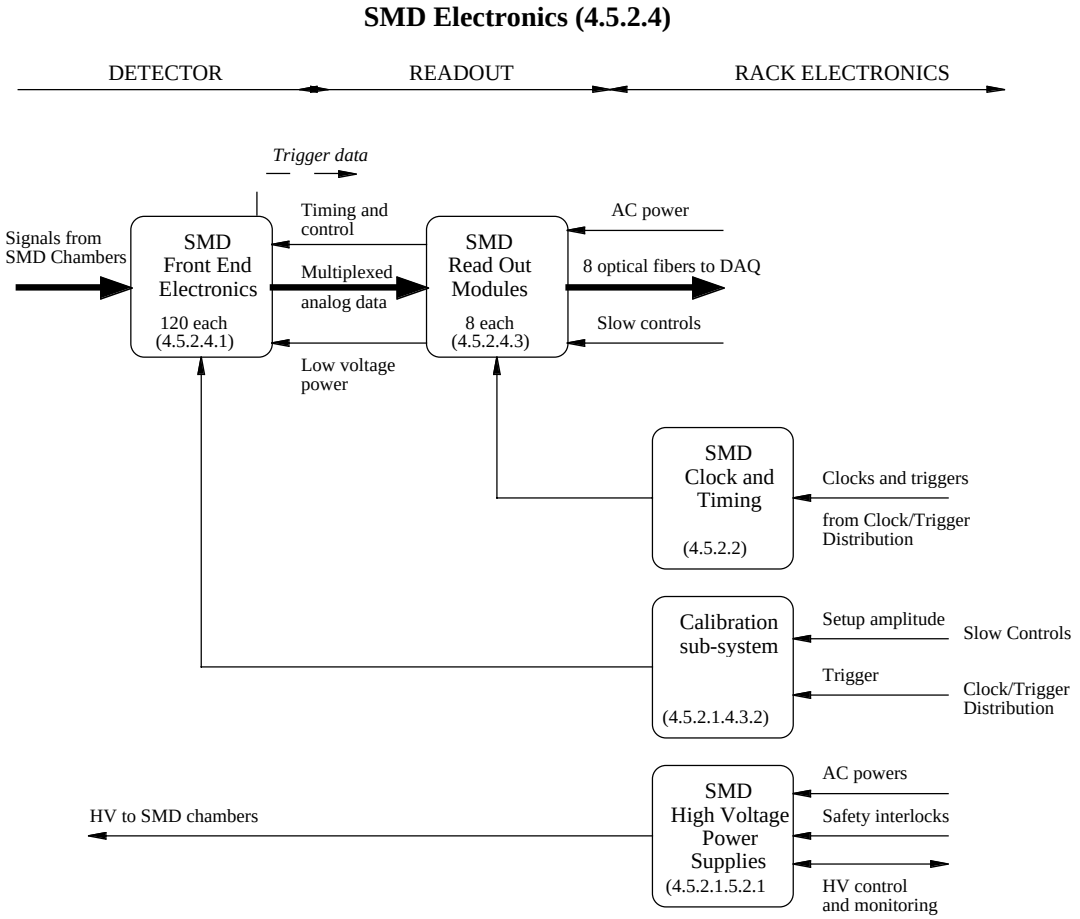


Fig. VII.17. More detailed layout of SMD electronics showing data path in bold.

As shown in Fig. VII.18, each FEE card has 300 wire inputs. Each input goes to one channel of the STAR Amplifier Shaper (SAS) chip where it is amplified and shaped. The SAS chip is an early development of a 16 channel chip that was developed for the STAR TPC as the "SAS16C" and is also used in the STAR MWPC Trigger detector. A production run of this part is currently under way for the MWPC. 15 of the 16 inputs are used on each of 20 SASs to match the wire count. The SAS characteristics are:

gain	24mV/fC
linearity	<4%
Internal calibration:	+/- 1%
Max output swing	2 Volts
Integrator dynamic range	>2.5pC
Shaping time(peaking)	60 to 150 ns
Tail correction	0.5 to 2 us
Crosstalk	<+/-0.36%
Equivalent Noise Charge in erms	

((Tp=80ns,Cboard=7.7pF = 560e + 13.7e/pF of detector capacitance.
(We expect 300 pF for the SMD).

Total power consumption	<750 mW
output load	50pF
die size	2.6 x 3.6 mm

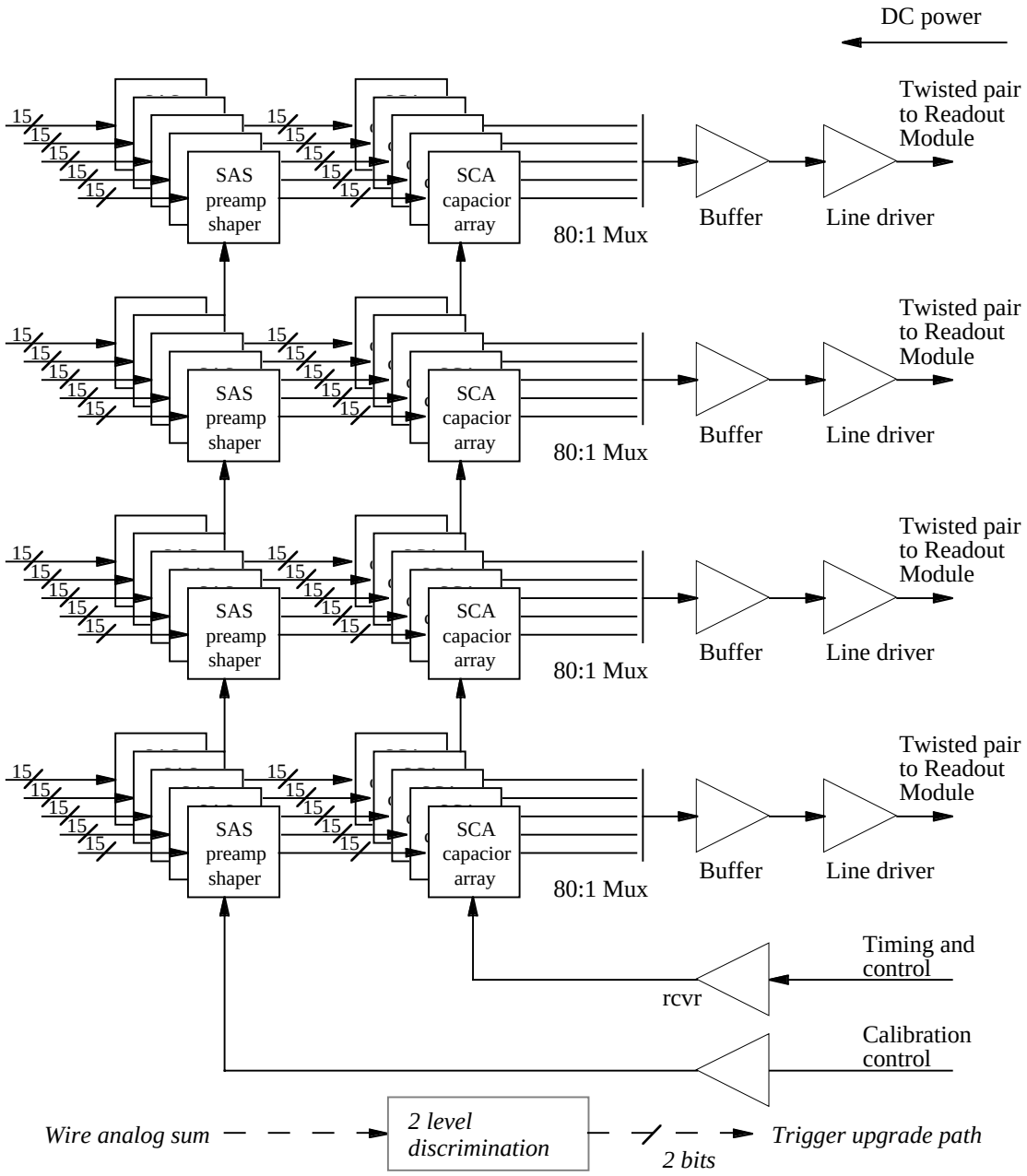


Fig. VII.18. SMD front end electronics showing the preamp/shapesr and switched capacitor arrays.

The output of the SAS is capacitively coupled to the inputs of the 16 channel Switched Capacitor Array (SCA). Capacitive coupling is used here to remove the pedestal variation of the SAS from the signal. The output DC bias of the SAS is settable

by external components for the SAS, but pedestal variation makes capacitive coupling necessary. For SMD operation, the output of the SAS will be from 1 to 3 Vdc This SCA was developed for the STAR Silicon Vertex Tracker (SVT) as "SVT SCA3". A production run for the SVT of this part is currently under way for the SVT. SCAs will be grouped in units of 5. 15 of 16 input channels on each device will be used. A total of 20 SCAs will be used on each FEE card. Details of the SC are shown in Fig. VII.19.

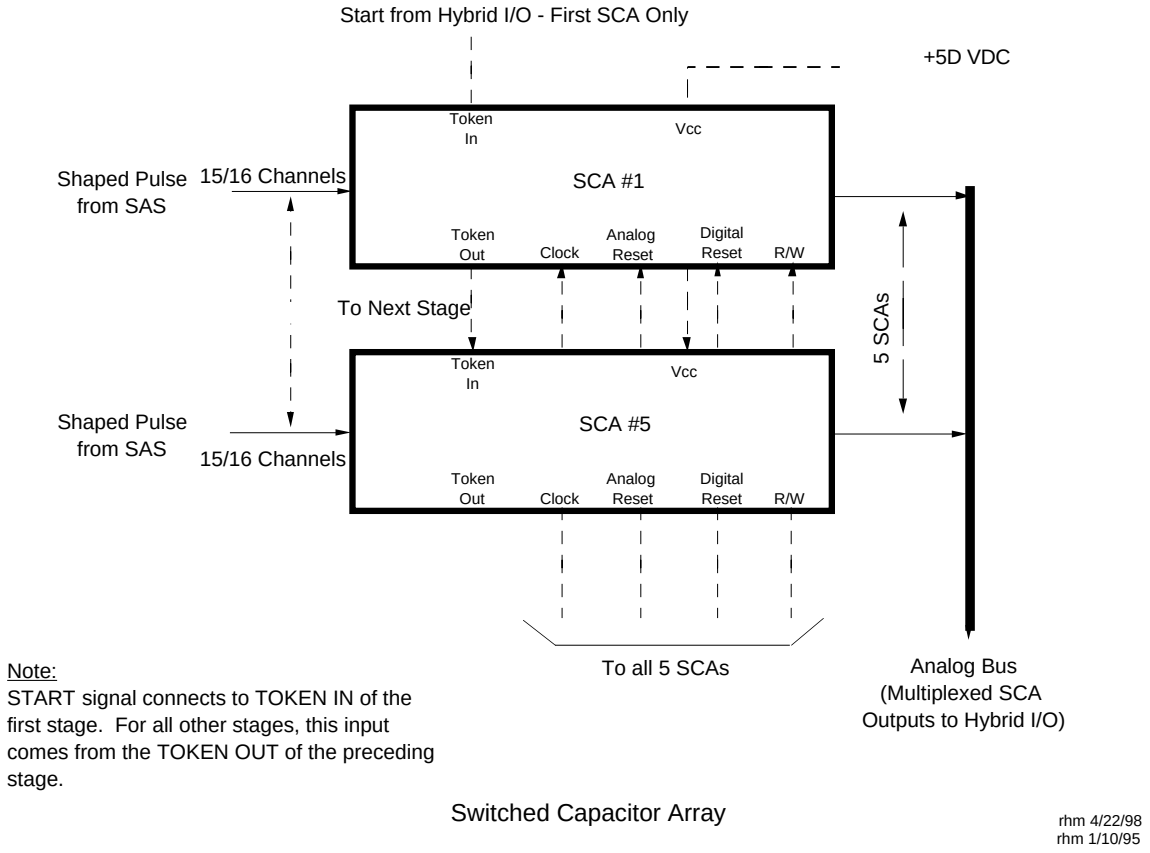
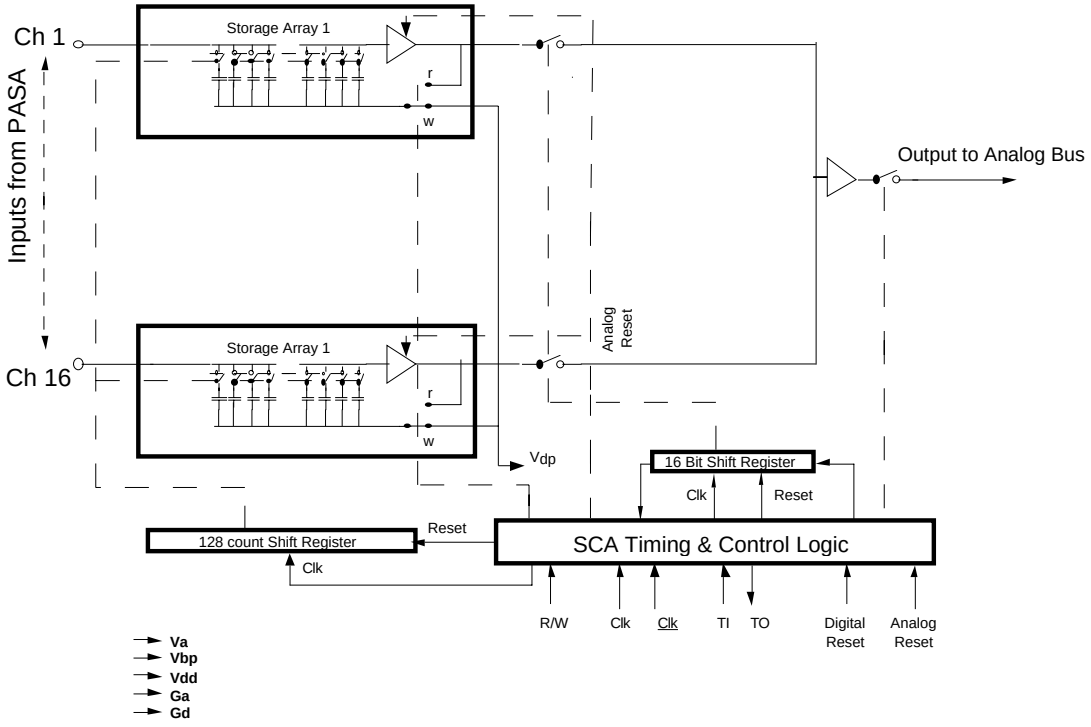


Fig. VII.19. Details of SCA used to read out SMD.

Input to the SCA will be biased externally for a 1 to 3 Vdc input range. The SCA output tracks the input at 1 to 3 Vdc. The SCA consists of 16 channels of circular buffers of 128 storage capacitors, buffer amplifiers and associated timing and control circuitry. The storage capacitors are sometimes called storage elements or pixels or cells or timebuckets. During operation, analog data are sampled and stored on each of the 128 storage elements in turn at a rate up to 3*RHIC strobe or 27 MHz. On the receipt of a trigger, the external clocking circuitry stops the acquire clock, switches from acquire to readout mode and a token is sent to the first SCA in each group of 5 to begin reading out the data. Data are read out channel by channel for the fist time bucket until all 16 have been read out. A token is then output from the first SCA that initiates the readout process in the next SCA. After all 5 SCAs have been read out, a new token is issued and the next time bucket is read out. The process repeats until the desired number of timebuckets has

been read out.

The SCA was designed for the SVT requirement of 128 storage elements or time buckets. The SMD needs only one sample stored. A peculiarity of the SVT makes the first time bucket read out unusable so two samples will be read out for the SMD. For the SVT, data acquisition stops immediately upon receipt of the trigger. For the SMD, dummy acquisition will continue until the readout is properly cued up. Two timebuckets will be read out, the first discarded and the second sent on to DAQ. Because the acquisition can take place at any of the 128 time buckets, calibration of pedestal offsets for all storage cells must and can be provided.



SCA Organization
(Switches shown in write state)

rhm
4/22/98

Fig. VII.20. Organization of the SCA used to read out SMD

The SCA characteristics are:

Gain	1.0 +/- 5%
Linearity	<1%
Max output swing	3 Volts
Crosstalk	<+/-1%
Noise	2.5 mVrms
readout rate	1 MHz
clock signal	pecl
output mux	up to 15 SCAs

Total power consumption	<150 mW
input capacitance	<10pF
die size	2.5 x 3.6 mm

The output of a group of 5 SCAs is multiplexed into a buffer and then into line drivers that send the multiplexed signals to the RDOs. The multiplexing is 80:1 but only 15 of each group of 16 channels is connected to a wire. The FEE cards also receive and distribute the calibration serial links and pulse for calibration via charge injection into the SASs.

Minimal electronics for a two level discriminator and input and output paths are provided for a future upgrade to a 2bit output from each FEE card to trigger.

Eight RDO modules will readout the SMD data. Four will be mounted at each end of the detector and will support 15 of the 120 FEE cards. Communication from FEE to RDO will be by twisted pair cables. The RDO module hardware uses cards previously developed for the STAR SVT. They consist of Analog and Memory Boards (AMB) used to receive and digitize input data, the Fiber Optic Board (FOB) which formats the data and sends it out to DAQ via the standard STAR fiber link (gigalink), and two variants of the Power and Timing Board (PTB and PTBa) which generate local timing and control signals, generate and distribute timing and control for the FEE cards, and provide voltage regulation for the power sent to the FEE cards. The RDO modules are shown in Fig. VII.21.

Each module is a self-contained replaceable module. In the event of a failure inside the module, the entire module will be replaced with a previously tested unit. The defective unit will be repaired on the bench. Debugging at the installed module is possible but will be avoided.

Each RDO will support 15 FEE cards including analog inputs, dc power for the FEE, and all timing and control signals except for calibration. Each RDO will have 3 PTB cards, 1 FOB and 5 AMB cards and an SMD specific I/O panel for cabling. The modules will use a standard 10 slot VME based crate with local power supply but does not use VME protocol on its backplane. Local cabling between cards supplements the backplane for certain signals. The RDO module receives input from 15 FEE cards as 60 multiplexed analog inputs. Input cables are routed through and I/O panel to the AMB boards for digitization.

AMB Inputs are differential and resistor packs on the card allow customization of the level and offset of the signals passed to the ADCs shifting the 1-3Vdc SCA signal levels to 0-2Vdc for the ADCs. The analog signals are digitized at 10bit resolution and temporarily stored in memory. The on card memory also allows storing an event for later read out by Slow Controls for diagnostic purposes as well as loading and retrieving test data.

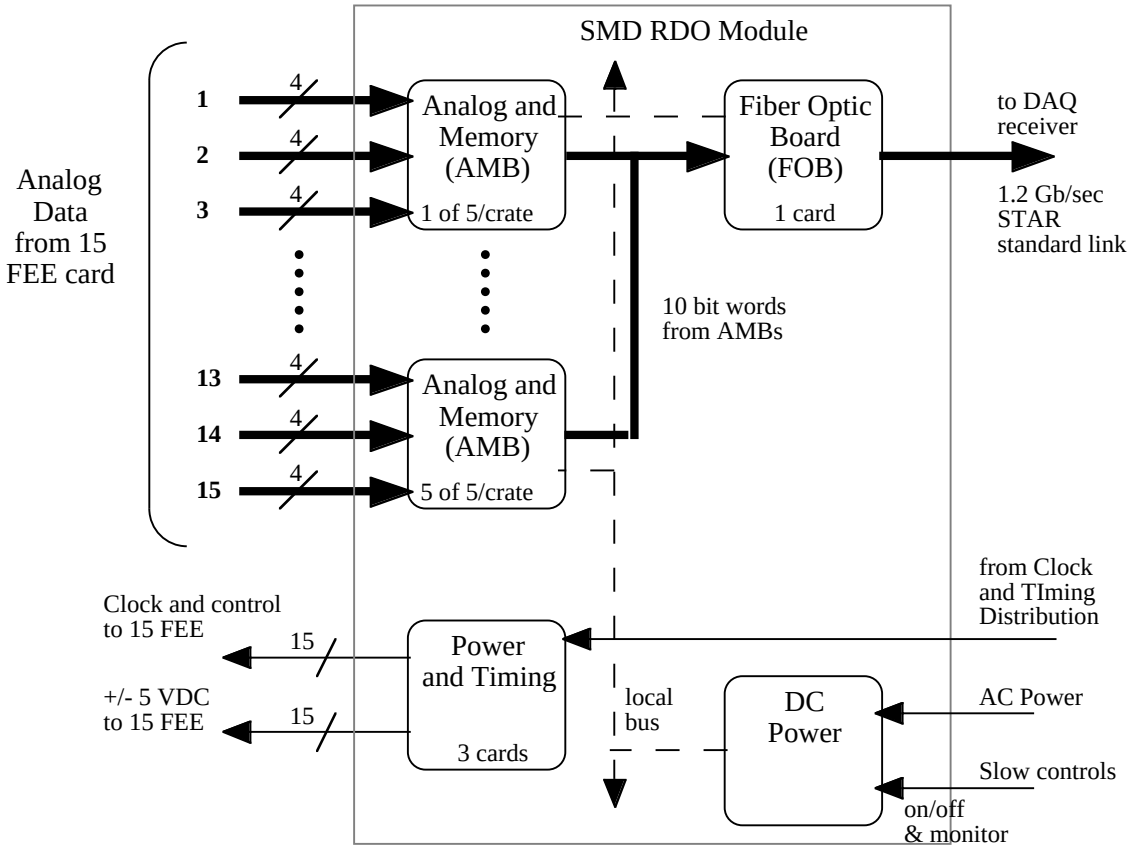


Fig. VII.21. SMD front end electronics showing the preamp/shapesr and switched capacitor arrays.

The data in memory is read out interleaved with the acquisition and transferred to the FOB board as two 10 bit words which are combined for the 20 bit transfer via gigalink to DAQ. The DAQ receiver buffers the data, does a pedestal correction and threshold zero suppression only.

VII.3 Trigger

VII.3.1 Trigger Overview

The EMC trigger is produced by the 150 tower readout cards located in 30 crates on the back-legs of the STAR magnet. The trigger information will be produced on each RHIC crossing and sent to data storage and manipulation (DSM) boards to be processed. These boards have been designed by the STAR trigger group and consists of programmable logic with 128 bits of input and 32 bits of output. An overview of the EMC/trigger interface is shown in Fig. VII.22.

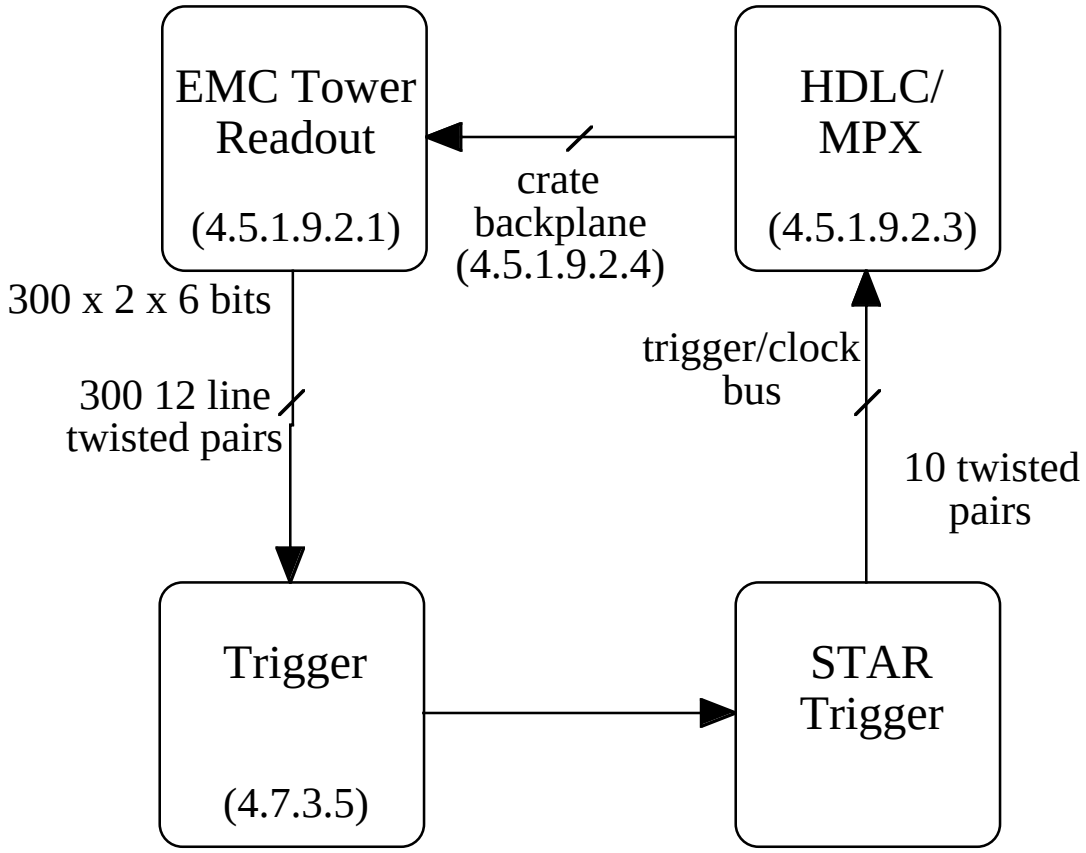


Fig. VII.22. Schematic layout of the EMC/trigger interface.

The EMC electronics will produce the following level-0 trigger information:

- 300 6-bit trigger towers
  - $(\Delta\eta, \Delta\phi) = (0.2, 0.2)$
- 300 6-bit high towers
  - $(\Delta\eta, \Delta\phi) = (0.05, 0.05)$

The trigger towers correspond to the sum of the energy deposited in 16 physical towers. The high towers contain the energy of the highest tower of the 16 towers making up a trigger tower. The EMC FEE produces 300 sets of 12 bit values that are sent over twisted pair cables to the DSM interface (DSMI) boards that convert the differential logic signals to the TTL logic signals required by DSM boards.

The inputs into the DSM (and corresponding DSMI) boards are grouped by η and ϕ to produce geometric sums. Each DSM is connected to 20 cables. 10 of these cables correspond to trigger towers and 10 to high towers. Each group of trigger towers and high towers in each DSM covers a geometric area of $(\Delta\eta, \Delta\phi) = (1.0, 0.4)$. This arrangement is illustrated in Fig. VII.23.

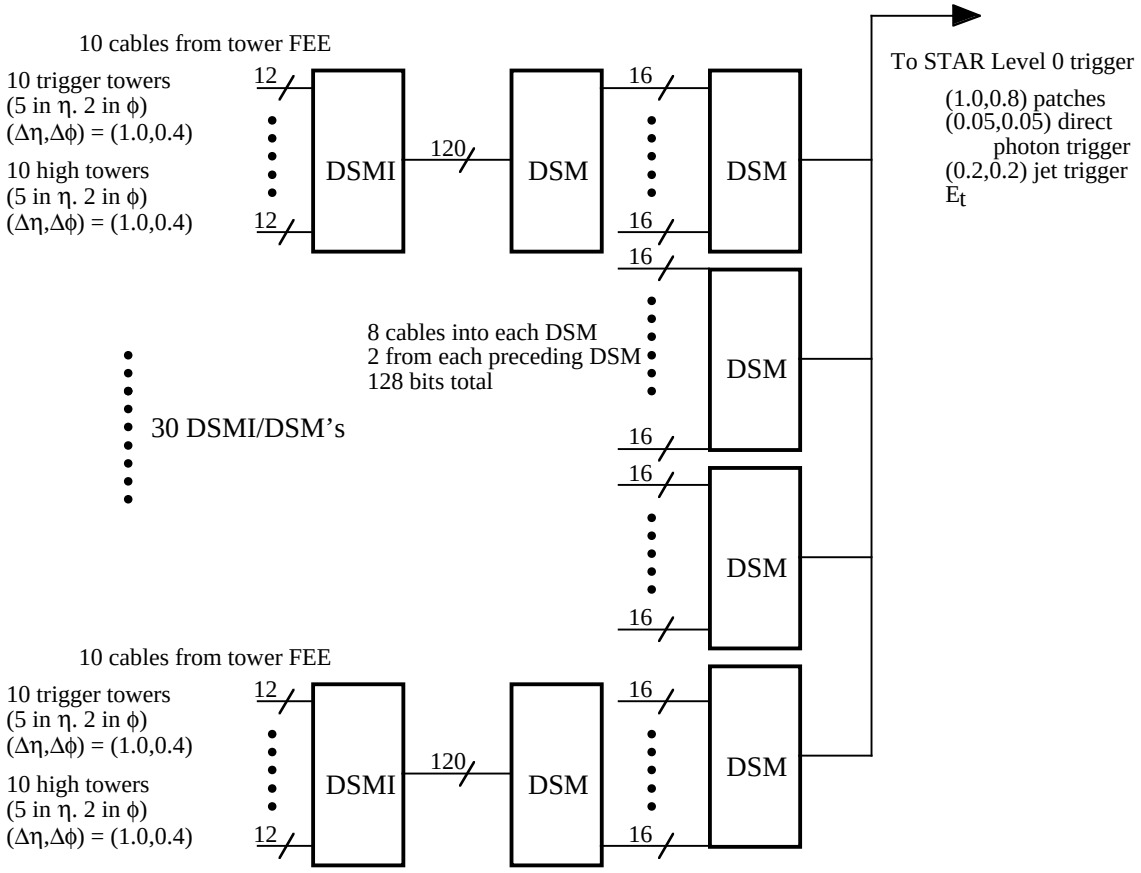


Fig. VII.23. Schematic layout of the EMC level 0 trigger.

The time to produce a level 0 trigger is 8 crossings in the tower FEE. Assuming that each layer of DSM boards can calculate in one RHIC crossing, the EMC level 0 trigger will be ready in 10 crossings to compare with the CTB. In 11 crossings, the EMC trigger will have produced all of its triggers.

- E_t, total transverse energy, in the EMC to be compared with the total charged particle multiplicity from the CTB
- (1.0,0.8) patches of transverse energy to be compared with the charged particle multiplicity from the same patches of the central trigger barrel (CTB)
- Direct photon trigger based on high towers
- Jet trigger based in trigger towers and (1.0,0.8) patches
- Two particle triggers

The EMC level 0 trigger requires 30 + 4 DSM boards to produce the basic trigger information. Correlation of this information with CTB will be accomplished by briding the inputs to the second layer of DSMs to the DSM tree of the STAR trigger based on the CTB. Two more DSMs in a third layer complete the EMC trigger by producing bits corresponding to triggers that involve only the EMC.

For example, a jet trigger can be produced based on thresholds on the highest trigger tower. Because the jet trigger rate at low p_t is larger than the rate desired at level 0, several thresholds must be defined. Placing a low threshold on the jet trigger allows

the measurement of low p_t jets that are necessary to understand the phenomena STAR is studying. These triggers must be scaled down to an acceptable rate. Putting a higher threshold on the jet trigger will select higher p_p jets at a lower rate but will also need a scale down factor. Finally, one places a threshold on high p_t jets that one wishes to accept always. This trigger is not scaled down.

Assuming that the EMC were allocated 3 bits in the STAR trigger word, the DSMs could be programmed to produce 8 different triggers. In some cases, the EMC could be allocated more bits and the corresponding number of triggers could be produced. These triggers can be scaled independently. Of course triggers involving the EMC and other detectors are produced by the STAR trigger (up to 2048 assuming that the 11 trigger bits are encoded by the DSM tree). Thus one could program several jets triggers, several direct photon triggers, and several multi-particle triggers.

VII.3 Interface to DAQ

The EMC electronics will send its data to DAQ over 9 gigalink fibers. One fiber is used to transmit the tower data and eight fibers are used to send the SMD data. The tower data collector will hold all recorded data tagged by the trigger token. On a level 2 accept, the tower data collector will push its data to DAQ. An interface card will reside in one of the TPC DAQ crates. This card will be designed by the STAR DAQ group. An upgrade path exists to send a copy of the tower data to all 24 TPC sector crates to allow level 3 trigger correlations between the EMC and the TPC tracks.

The SMD read out cards also hold the accepted data until a level 2 accept is received. The SMD read out boards then send the SMD data to a DAQ receiver that is to be designed by the STAR DAQ group.

VII.4 Dynamics Range Requirements for the SMD

The search for the direct photons candidate and detection of electrons from W and Z^0 decay lead us to measurement of electromagnetic showers with energy varying from 0.5 GeV to 60 GeV. The low end comes from looking for low energy gammas from the asymmetric π^o decays that can fake direct gammas. The measurement of 0.5 GeV electromagnetic showers means the detection of minimum-ionizing particles in the SMD with reasonable efficiency will be needed. The fluctuation of the ionization from MIPs in thin layers of gas finally defines the low threshold that is equivalent to 0.125 keV in terms of total ionization for a Ar/CO_2 gas mixture. Monte Carlo calculation show that the total ionization will be ~160 keV in a single channel of the SMD (central strip) from a 60 GeV electromagnetic shower. This number lead us to an overall dynamic range of 1:1240.

Monte Carlo calculations shows that the reasonable signal to noise ratio for the direct photon is expected for the P_t region form ~12 GeV up to 25-30 GeV. Above 30 GeV the main function of the SMD will be the improvement of the overall hadron

suppression power for the non-segmented EMC. The high P_t charged hadrons that can be misidentify as electrons is expected to be the most serious source of background. The information from SMD placed at depth 5 X_0 will allow to reduce the level of background (remaining after the selection of the events using TPC and EMC information) in 1.5-2 times, as was calculated in the Monte Carlo.

The invariance of the transverse shower profile in the energy region from ~7 GeV up to 150 GeV allows us to make the identification of electron/photon candidate using the tail distribution in the transverse shower profile even in case when the 'central' strip is saturated. This means that the effective dynamic range needed for the SMD is close to 1:640. The proposed STAR Amplifier-Shaper (SAS) for the SMD readout includes a pole/zero network which cancels the long ion tile. A pole/zero T bridge network in shaper's feedback loop was designed with controlled externally MOS resistor to adjust the tail cancellation depending on the gas mixture in the TPC. The two mixtures P10 and He-Eth was considered in the SAS shaper design.

The gas mixture in the SMD is Ar-CO_2. The signals arising from the avalanche region is approximated by a 1/t relationship and the total collection time for the Ar mixture expected to be close to ~30 μs. For SMD gas mixture the shape of the signal arising from the avalanche region will be different compare to shape of signal for the TPC gas mixtures. The rise time expected to be close to ~50 ns, and the ion tail falloff will be in between the ion tails for the P10 and He-Eth mixtures. (This statement is based on extrapolation of the data for the Ar/CH4 (80%/20%) gas mixture , see T.Akesson et al. NIM A361(1995)) The current design of SAS make it possible to optimize the shaping of the SMD signals to achieve the optimal relation between peaking time and noise. The test measurements with the first full scale operational chamber will be needed, and we expect they will be accomplished during the summer 98, prior the next test run in October 98.